Microprocessor and method for selectivity excution prefetched instruction

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A microprocessor that selectively performs prefetch instructions based upon an indication of future processor bus activity and cache line status. The microprocessor includes a programmable threshold register for storing a threshold value. The threshold value is such that if the depth of bus requests queued in the bus interface unit of the microprocessor is greater than the threshold value, this condition indicates a high likelihood of a high level of bus activity in the near future, for example due to a workload change. If a prefetch instruction cache line address misses in the processor cache, then the line is not prefetched from external memory unless the line may be supplied from one level of internal cache to a lower level of internal cache. However, even in this case the line is not transferred internally if the line status is shared.